Shielding and Electrical Performance of Silicon Sensor Supermodules

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HIGH resolution tracking and efficient, precise secondary vertex detection are crucial requirements in modern particle physics experiments. Detectors based on silicon pixel or microstrip sensors are capable of providing excellent position resolution of the order of 1 to 10 μm. In addition silicon sensors can be made extremely radiation tolerant and can be operated at high readout frequencies. An extremely harsh radiation environment, high beam collision rates, and the need for high resolution are characteristic for high-luminosity hadron colliders. Silicon tracking detectors have become a part of virtually every modern hadron collider experiment, and increasingly larger silicon based detector systems are being operated and designed.

In order to exploit the high intrinsic hit resolution of silicon sensors, multiple scattering must be minimized by maximizing the radiation length of the detector. Thus the detector systems must be lightweight and preferably be composed of materials with low atomic number. Another challenge is that fluences of 10^{14} or 10^{15} particles/cm^2 cause substantial radiation damage in bulk silicon and increase sensor leakage current. To avoid thermal run-away and to minimize leakage current and shot noise, the sensors must be cooled actively. However cooling pipes and coolant increase the detector material, and make it more difficult to minimize multiple scattering. Ideally pixel detectors or double-sided microstrip sensors (sensors that are patterned on the top and bottom sides) are used to obtain a 2-dimensional spatial measurement. If instead two single-sided microstrip detectors are combined, the sensor material is further increased. Mounting structures and cables for data and control signals, and power also add substantially to the overall material balance.

The above constraints make the design of a silicon detector system a challenging packaging problem. Given the readout chips and the silicon sensors, different designs of the overall system may lead to very different performances and have major advantages or disadvantages for assembly, production and total cost.

An elegant packaging solution which addresses the above constraints was found in the design of the CDF silicon detector [2], [3] for the (now canceled) Run IIb of the Tevatron accelerator. The main building block of the detector is a "supermodule" or stave, a highly integrated mechanical, thermal, and electrical structure. Fig. 1 shows a photograph of a supermodule inside a protective box. The supermodule has 3072 electronic channels, is 66 cm long, and weighs only 156 grams. Its core is composed of carbon fiber, foam, and cooling tubes. The supermodule carries single-sided silicon microstrip sensors on its top and bottom sides. A Kapton/copper/aluminum flexible circuit laminate ("bus cable") provides power, high voltage, and
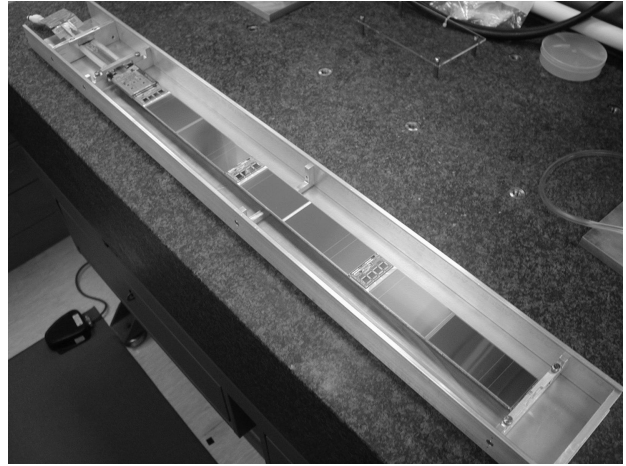

Fig. 1. Picture of the stave top side. The bottom side is also equipped with silicon sensors and hybrids.

data and control signals. It is glued directly under the silicon sensors. The hybrids carrying the SVX4 readout chips [4] are glued on top of every other sensor. For further information see [5].

The compact arrangement of service cables, sensors and readout electronics simplifies supermodule production and assembly tremendously. It's also very cost efficient. The stave is self-supporting and is attached on both ends at a bulkhead. It is read out on one end only, so that two staves supported by three bulkheads form a detector of 2 x 66 cm length. This arrangement looks attractive for future silicon systems in the context of a possible LHC upgrade.

The proximity of the bus cable to the silicon sensors makes pickup of bus cable activity into the silicon sensors more likely, and the suppression of this effect requires particular care. This is even more important if the detector is operated in deadtimeless mode with data acquisition continuing during digitization and readout. Critical effects are the possible coupling of the digitization and readout activity into the analog (preamplifier and pipeline) section of the readout chip and the coupling of the control and data signals into the silicon sensor.

The basic coupling mechanisms and the measured performance of a prototype supermodule are discussed in [6]. In the current paper, we present the performance of the final supermodules.

The performance of a supermodule in deadtime-less operation is illustrated in Fig. 2. The figure shows the ADC counts recorded for an arbitrary channel as a function of time/mode of chip operation: first when the the back-end section of the chip is idle; second while it is digitizing; third while it is

reading out. Each data point corresponds to a different charge integration period ("bucket") and can be uniquely associated with a given sequence of the control signals. In the absence of a signal caused by a particle or of electromagnetic interference, the channel should be at a constant pedestal value with fluctuations around this value mostly due to the noise of the chip preamplifier. Indeed the few systematic shifts seen in the figure are much smaller than the signal that would be produced by a minimum ionizing particle (MIP). The observed performance is very satisfactory.
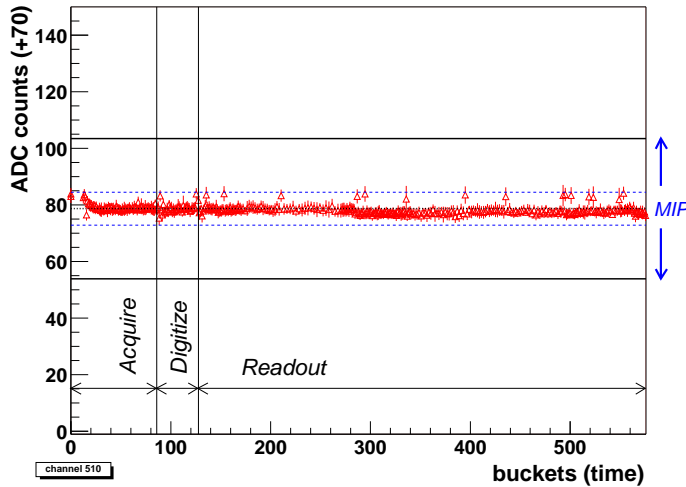

Fig. 2. Illustration of deadtime-less supermodule performance.

An interesting phenomenon, which was not discussed in [6], is the presence of local electromagnetic interference through the (grounded) aluminum shield. This effect is illustrated in Fig. 3, which shows the pedestal seen at all strips at a given moment in time. The colored vertical bands correspond to the bus cable traces below the corresponding channels. Power traces are wider and are thus covered by more strips/channels. Clock, data, and control lines are narrow (75 μm width) and are covered by one strip only (readout strip pitch is 80 μm). The bottom curve of the figure shows a significant interference structure which is caused by the front-end clock (LVDS) signal which runs under the microstrips associated with the channel numbers close to 200. The size of the interference structure scales with the front-end clock driver current, which was set to its maximum value in this case in order to study the effect best.

Doubling the shield thickness from 25 μm to 50 μm suppresses the front-end clock interference completely. The reduction is larger than expected from the skin effect alone. Heavy shielding of the supermodule is prohibitive due to the constraints on the radiation length. Understanding of the minimum shielding requirements is thus crucial for the design of the supermodule. Similar effects are seen for the interference signals due to data and single-ended (CMOS) control signals.

We present the electrical performance of the final supermodules. We also discuss the effectiveness of the shielding and other
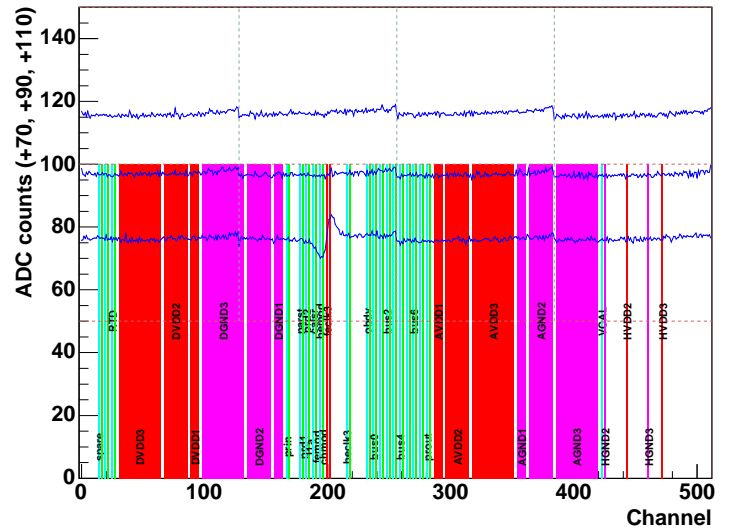

Fig. 3. Stave pedestals recorded for a supermodule with a 25 μm thick aluminum (bottom curve); with a 50 μm thick shield (middle curve); and for a supermodule sensor without underlying bus cable traces (top curve). (The vertical dashed lines separate channels read out by different SVX4 chips.)

noise reduction techniques and compare it with quantitative analytical and numerical calculations, for different readout frequencies and supermodule geometries. Our results are relevant for the design of future silicon systems, in particular at high-luminosity hadron colliders such as the SuperLHC [7]. Similar shielding problems occur in areas other than particle instrumentation as well [8].

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